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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,924	12/15/2003	Yasuhiro Ikarashi	9281-4673	5834

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Brinks Hofer Gilson & Lione
P.O. Box 10395
Chicago, IL 60610

EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,924	IKARASHI, YASUHIRO	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-21,23-26 and 29* is/are rejected.

7)☒ Claim(s) *3, 4, 22, 27, 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12-15-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Segawa et al. 6,342,818 (Segawa).

Figure 14 of Segawa discloses a signal generator having a voltage controlled oscillator (VCO) 15 (means for generating an oscillation signal) wherein the input terminal shown in Figure 14 for the VCO forms a control voltage input terminal for inputting an external control voltage for determining the frequency of the oscillation signal from the VCO. Note that the loop filter 14 that produces the external control voltage is an "external circuit" (See column 18, around line 33). Thus the signal that the loop filter 14 produces and provides to the control voltage input terminal is an "external control voltage". Element 16 of Segawa forms a frequency divider circuit (means for frequency dividing the oscillation signal) that is connected to the output of the VCO. Element 16 also clearly divides the "oscillation signal output from the voltage controlled oscillation circuit". The output terminal of element 16 of Segawa (means for outputting a frequency divided signal) forms the so-called "frequency divided signal output terminal". This terminal is clearly "for outputting a frequency divided signal output from the frequency divider circuit" as clearly illustrated by Segawa.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21, 23, 25, 26 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vandegraaf 4,347,484 (Vandegraaf) in view of Norimatsu 5,173,665 (Norimatsu).

Figure 10 and the relevant text of Vandegraaf discloses a signal generator having voltage controlled oscillation circuit 206 (means for generating an oscillation signal), a means for dividing the oscillation signal composed of elements like 208, 210, 212 and 214 and a means for outputting a frequency divided signal (Note the output terminal of the above mentioned frequency divider element.). The loop filter forms part of a first control means that controls the frequency of the oscillation signal in the well-known manner. The structure noted above also provides for a method of generating a signal. Most of the claimed method steps are merely a description of the functionality of the structure of the prior art, for example "generating a voltage controlled oscillation signal" is what a voltage controlled oscillator does. The signal that is applied to the phase comparator 202 of Vandegraaf is of a "wide frequency range". It is noted that applicant has not defined what applicant specifically means by "wide frequency range", thus a fair and reasonable reading would include the frequency range of Vandegraaf. The examiner must give the broadest reasonable interpretation of the claims (See MPEP 2111.). Vandegraaf lacks the controlling or is silent on the controlling of the frequency division ratio by a second control means. The frequency divider of Vandegraaf is clearly composed of cascading means for frequency dividing as shown in Figure 10 thereof.

Figure 1 of Norimatsu discloses that it is well known in the art to control the frequency division ratio by a second control signal generating means(unshown) that outputs a signal D so as to allow for the adjustment of this ratio which will vary the output frequency of the voltage controlled oscillator 22. This will form a structure commonly called a frequency synthesizer or the like. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided Vandegraaf with frequency dividers that are adjustable in frequency divisions ratio by a second so as to enable adjustment of the frequency division ratio as taught by Norimatsu. One of ordinary skill in the art would have been additionally motivated to make the combination as this allows for the frequency range to be adjusted as taught by Norimatsu. Norimatsu is silent on whether the signal D is internal or external, but the claims of the instant applicant do not recite what the signal that controls the frequency division ratio is external to. Therefore a reasonable reading of the claims would be that the signal D is external as it comes from an unshown second control signal generating means that is outside the circuit shown in Figure 1 of Norimatsu. Alternatively, a frequency synthesizer is commonly known to have it modulation input or frequency-changing input obtain a signal from an outside source such tuning dial on a radio. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized an external signal to control the frequency divider because, as the Norimatsu and Vandegraaf references are silent on the details of the second signal source one of ordinary skill in the art

would have been motivated to use any art-recognized equivalent source such as the conventional external second signal source including the "tuner" on a radio.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vandegraaf 4,347,484 (Vandegraaf) in view of Norimatsu 5,173,665 (Norimatsu) as applied to claims 21, 23, 25 and 26 above, and further in view of Segawa et al..

Vandegraaf is silent on whether the loop filter is internal or external. The claims are not specific what is external, however, Segawa in column 18, around line 33 thereof clearly points out that the loop filter can be internal or external. Thus, Segawa clearly points to the art-recognized equivalence of these two arrangements. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilize an external filter 204 in Vandegraaf given the art recognized equivalences of these two arrangements. Besides being motivated by the art recognized equivalence, one of ordinary skill in the art would have been additionally motivated to make the combination because capacitor elements takes up a lot of space on an integrated circuit and in order to save integrated circuit space it is common known to make the loop filter external to the rest of the circuit.

Claims 1, 5-8, 10-12, 14-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vandegraaf 4,347,484 (Vandegraaf) in view of Segawa et al. 6,342,818 (Segawa).

Figure 10 and the relevant text of Vandegraaf disclose a signal generator having voltage controlled oscillation circuit 206 wherein the input of element 206 forms a control voltage input terminal. Vandegraaf fails to call the signal applied to this control voltage input terminal "an external signal". However, it is well known that the loop filter 204 of Vandegraaf can be an external component. Segawa in column 18, around line 33 thereof clearly points out that the loop filter can be internal or external. Thus, Segawa clearly points to the art-recognized equivalence of these two arrangements. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilize an external filter 204 in Vandegraaf given the art recognized equivalences of these two arrangements. Besides being motivated by the art recognized equivalence, one of ordinary skill in the art would have been additionally motivated to make the combination because capacitor elements takes up a lot of space on an integrated circuit and in order to save integrated circuit space it is common known to make the loop filter external to the rest of the circuit. Figure 10 and the relevant text of Vandegraaf also clearly disclose a frequency divider circuit composed of cascaded frequency dividers 208, 210, 212 and 214. This does as the name implies it frequency divides the oscillation signal (Input signal to the frequency divider combination.). The output terminal of this frequency divider combination clearly is "for outputting a

frequency divided signal output from the frequency divider circuit". The division ratio as meant by Vandegraaf is a whole number (N_1 X N_2...). However, fractional dividers are also conventionally known so as to divide the frequency via a fractional number. Accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a fractional divider given that these are conventionally known to those of ordinary skill and are known by those of ordinary skill to offer a finer range of control in the frequency divider circuit. One of ordinary skill would have been motivated to make the combination so as to allow for greater control over the frequency divided signal since one is using a fractional number as is conventionally known in the art. Figure 10 of Vandegraaf clearly points out that the frequency at the output of the frequency divider arrangement is equal to or lower than the frequency of the oscillation signal. Note that F_{OUT} is higher than F_{OUT} divided by the frequency divider ratio i.e. N_1 X N_2... .

Column 18 of Segawa as noted above clearly points out that the loop filter can be integrated along with items like the phase comparator, frequency divider and the charge pump or the loop filter can be formed external to these items. Vandegraaf and Segawa are silent on the integration of the VCO along with the frequency divider. However it is obvious to those of ordinary skill to integrate a circuit so as to form a more compact and durable structure. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have integrated the VCO along with the frequency divider circuit so as to from a more compact and durable structure as is well known in that art. One of ordinary skill would have been motivated to make the combination so as to make the circuit structure more compact and more durable. Note that the integration of the circuit as noted above includes the integration of the terminals, i.e. nodes of the circuit. In other words the integrated circuit is provided with the control voltage input terminal and the frequency division signal output terminal with these terminals being internal to the integrated circuit.

With respect to claims 6 and 8, claim 6 recites a FET functioning as a voltage controlled variable capacitor and claim 8 recites that the VCO "employs field effect transistors". Note that a FET functioning as a voltage variable capacitor is still a "field effect transistor". VCO's that employ voltage controlled capacitors such as FETs are conventionally known art-recognized equivalent structures in the art. This is merely reciting an art recognized equivalent VCO circuit. Likewise claims 11 and 12 recites another conventionally known art recognized equivalent VCO structure, namely a VCO that has a varactor diode in a resonant circuit coupled to a base of an oscillating transistor.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the VCO of Vandegraaf with one that has a FET functioning as a voltage controlled variable capacitor or with a one that has a varactor as the frequency controlling element because as the Vandegraaf reference is silent on the details of the VCO one of ordinary skill in the art would have been motivated to use any art recognized conventional VCO such as the conventional VCO that employs a FET as a voltage controlled variable capacitor.

Vandegraaf and Segawa are both silent on the use of "CMOS technology" to form the integrated circuit. Applicant does not define "CMOS technology" specifically in the specification and thus it common and usual meaning has been used. CMOS technology refers to the technology of forming semiconductor devices and is merely the forming of things like diffusion regions etc.. Using CMOS technology necessary mean that CMOS transistors are formed. Applicant does not claim that CMOS transistors make up the VCO or the frequency divider, just that "CMOS technology" is used to form the integrated circuit. Note that the examiner must give the broadest reasonable interpretation to the claims (See MPEP 2111). Since the final product as noted above, namely an integrated circuit is formed which would include regions of both p and n conductivities; it is an obvious consequence that the final product would have both p and n conductivities. However, VCO's that employ CMOS transistors are conventional art recognized equivalent VCO structures. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have employed a CMOS based VCO which would be a VCO that is formed using CMOS technology because, as the Vandegraaf and Segawa references are silent on the exact structure of the VCO circuit one of ordinary skill in the art would have been motivated to use any art recognized equivalent VCO structure including conventional VCO's that employ CMOS transistors.

With respect to claims like claim 10 Vandegraaf is silent on the use of a circuit board on which to make the circuit of Figure 10. One common well known conventional way to form a circuit is on a circuit board with the terminals of the circuit being provided on the end faces or the underside of the circuit board. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the circuit of Vandegraaf and Segawa on a circuit board with the terminal contacts provided on the end faces or the underside of the board because as the Vandegraaf reference is silent on the exact structure used to form the circuit one of ordinary skill in the art would have been motivated to use any art-recognized equivalent means to form the circuit such as the conventional circuit board having the terminals provided on the end faces or the underside of the board. One of

ordinary skill in the art would have additionally been motivated to form the circuit of Vandegraaf in combination with Segawa on a circuit board so as to provide support for the circuit elements.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vandegraaf 4,347,484 (Vandegraaf) in view of Segawa et al. 6,342,818 (Segawa) as applied to claims 1, 5-8, 10-12, 14-18 and 20 above, and further in view of Hajimiri et al. 6,867,656 (Hajimiri).

Figure 1A and the relevant text of Hajimiri teaches that is well known to provide a buffer between the oscillator and the frequency divider. Since Hajimiri does not specifically point to a reason for the buffer, the reason must be the conventionally known reason why one of ordinary skill utilizes a buffer in a circuit. It is common knowledge to those of ordinary skill that a buffer is used in circuits to provide isolation between two elements and to provide sufficient drive to the elements downstream the buffer.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a buffer between the oscillator and the frequency divider of Vandegraaf so as to provide for isolation between the oscillator and the frequency divider and so as to provide for sufficient drive for the frequency divider as taught by 'Hajimiri,

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vandegraaf and Segawa as applied to claims 1, 5-8, 10-12, 14-18 and 20 above, and further in view of Brunn et al. 6,650,195 (Brunn).

Vandegraaf and Segawa both seem to be directed to a single ended signal arrangement i.e. Vandegraaf and Segawa are silent on the voltage controlled oscillator having a balanced output. However, to utilize the same circuit in a balanced arrangement or an unbalanced arrangement is common engineering practice. Note Figure 2 of Brunn.

Thus it would have been obvious to make the invention made obvious by Vandegraaf and Segawa in a balanced arrangement since it was known in the art that circuits can be formed in either unbalanced configurations or balanced configuration as taught by Brunn.

Claims 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vandegraaf and Segawa as applied to claims 1, 5-8, 10-12, and 14-18 above, and further in view of Norimatsu 5,173,665 (Norimatsu).

Vandegraaf and Segawa are silent on the use a variable frequency divider controlled by a second control circuit.

Figure 1 of Norimatsu discloses that it is well known in the art to control the frequency division ratio by a second control signal generating means(unshown) that outputs a signal D so as to allow for the adjustment of this ratio which will vary the output frequency of the voltage controlled oscillator 22. Note that signal D is a "switching signal" as this switches the frequency-dividing ratio. The structure of Norimatsu will form a structure commonly called a frequency synthesizer or the like. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided Vandegraaf with frequency dividers that are adjustable in frequency divisions ratio by a second so as to enable adjustment of the frequency division ratio as taught by Norimatsu. One of ordinary skill in the art would have been additionally motivated to make the combination as this allows for the frequency range to be adjusted as taught by Norimatsu. Norimatsu is silent on whether the signal D is internal or external, but the claims of the instant applicant does not recite what the signal that controls the frequency division ratio is external to. Therefore a reasonable reading of the claims would be that the signal D is external as it comes from an unshown second control signal generating means that is outside the circuit shown in Figure 1 of Norimatsu. Alternatively, a frequency synthesizer is common known to have it modulation input or frequency-changing input obtain a signal from an outside source such tuning dial on a radio. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized an external signal to control the frequency divider because, as the Norimatsu and Vandegraaf references are silent on the details of the second signal source one of ordinary skill in the art would have been motivated to use any art-recognized equivalent source such as the conventional external second signal source including the "tuner" on a radio.

Claims 3, 4, 22, 27 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after .

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
June 13, 2005

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817